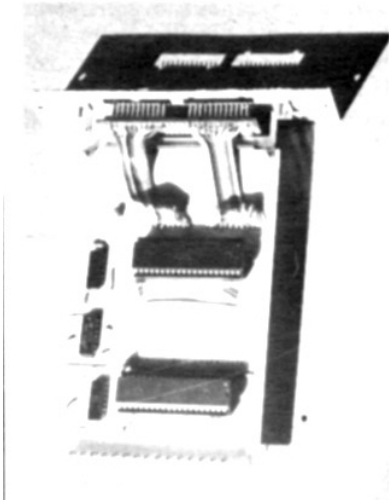


PARALLEL INPUT AND OUTPUT

VIA 6522 and PIA 6820

H. J. C. Otten



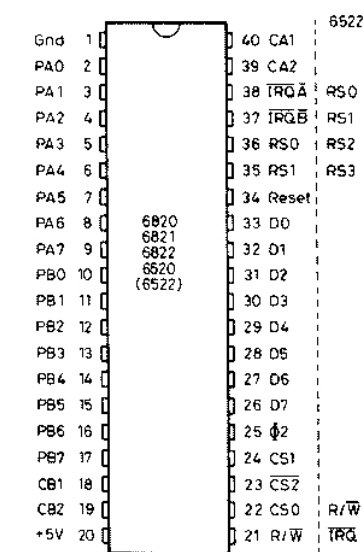
The subject of this article is a family of parallel input/output ICs: the PIA 6820, 6821, 6520 and the VIA 6522. These are widely used ICs, and not only in 6500 and 6800 microprocessor systems. Besides the general hardware characteristics of the PIA and the VIA, a practical implementation is presented.

The PIA (Peripheral Interface Adapter) and the VIA (Versatile Interface Adaptor) are suitable building blocks in a microprocessor system for various input and output lines. The VIA is a much more powerful IC than the PIA. Both ICs provide two sets of eight input or output lines under full program control, plus a number

of control lines that allow, for example, data transfer between a peripheral device and the processor. In addition, the VIA has two programmable timers and a shift register.

Despite these differences, the PIA and the VIA are almost pin-compatible. This can be

Afb. 1 Aansluitgegevens van een PIA en een VIA.



seen in fig. 1. The pinouts show that we are dealing with members of the 6500 and 6800 families. The ICs can be connected without problems to the buses of 6502, 6800 and 6809 microprocessors. With somewhat more effort, the PIA and the VIA can also be used in other microprocessor systems.

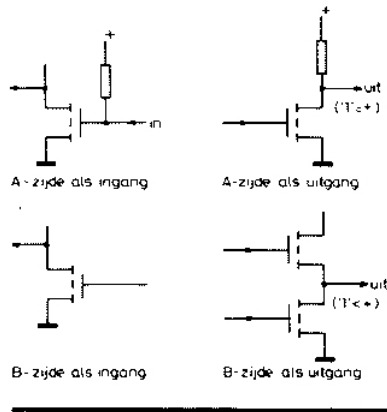
Microprocessor interface

The following signals are needed for communication with the microprocessor:

- 8-bit data bus, D0 through D7.
- E clock signal, often called $\phi 2$. Depending on the type, for example the 68B20 for 2 MHz, this is the clock signal.
- Select inputs. The PIA has three select inputs: CS0 and CS1 must be true and CS2 must be false to address the PIA. The VIA lacks CS0.
- Register select inputs. The PIA occupies four

addresses; the VIA has 16 register addresses. The VIA therefore has four register select inputs, RS0 through RS3, and the PIA has two: RS0 and RS1.

- Control signals such as R/W and RESET, and two IRQ interrupt outputs, one for each of the two 8-bit input/output ports. IRQA and IRQB are open-collector outputs.
- Supply lines for ground and +5 V, with a maximum current consumption of 100 mA.



Inputs and outputs

Both the VIA and the PIA have two input/output ports of 8 bits each: the A side and the B side. The inputs/outputs of the A side are PA0 to PA7 and those of the B side PB0 to PB7. The A and B sides of the PIA differ in their electrical characteristics. The A side is fitted with a pull-up resistor and presents a TTL-comparable load as an input line. As an input, the B side behaves as a tri-state input. When programmed as outputs, both the A and B sides can drive TTL levels. The B side is suitable for directly driving the

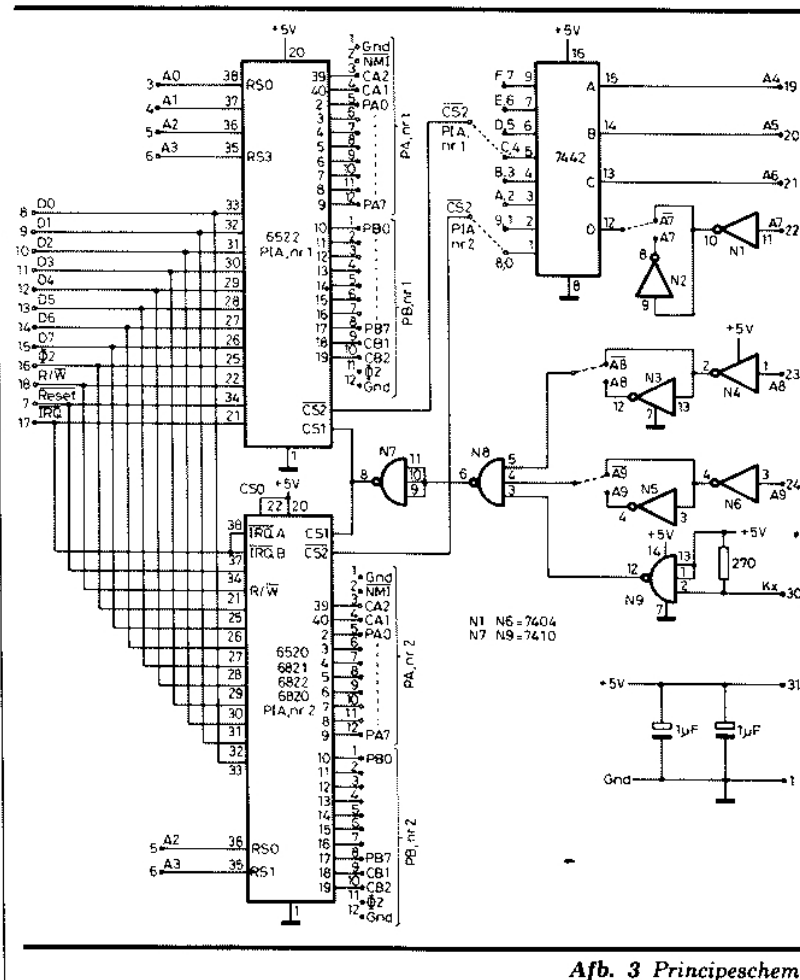
base of a transistor.

Fig. 2 shows what causes the differences in electrical characteristics. The A side is usually used as input, because without additional measures the B side has an undefined value when used as input. The pull-up resistor on the A side ensures that an undriven input is high. Considerations of this kind are important in preventing malfunctions. If, for example, the device connected to the PIA fails, the PIA input on the A side is high and on the B side undefined. The B side is usually more suitable as output because of its better drive capability.

Control lines

Both the VIA and the PIA have two control lines per port. The lines for the A side are CA1 and CA2, and for the B side CB1 and CB2. The characteristics of the control lines are not entirely the same for the PIA and the VIA, and there are also differences between the A and B sides. Discussion of the control lines is therefore postponed for now.

Electrically, the control lines are TTL-compatible.



Afb. 3 Principeschema.

Practical design

A practical design has been made for experimenting with the PIA and the VIA. Fig. 3 shows the schematic diagram. The near pin-compatibility of the PIA and the VIA was already mentioned in the introduction. This design takes advantage of it: one schematic and one PCB layout serve every combination of a PIA and a VIA, with a maximum of two per card. By choosing a few wire jumpers, the IC socket is made suitable for either a PIA or a VIA. The component layout of fig. 5 and the schematic therefore include a PIA (PIA no. 1) and a VIA (PIA no. 2) to show the difference. This is not essential; by fitting the appropriate wire jumpers (marked IRQ and R/W on the component layout), two PIAs or two VIAs can be installed.

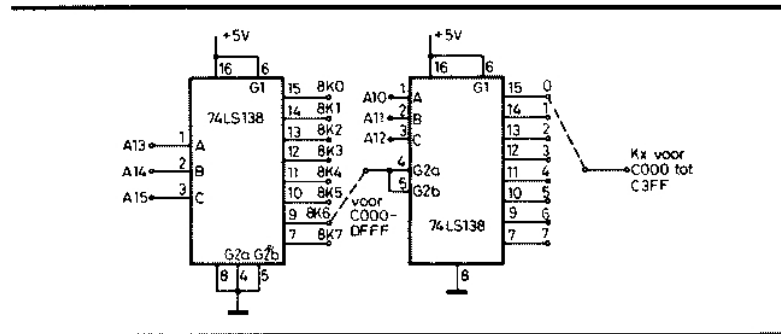
Apart from the two PIAs or VIAs, the schematic shows little else. The remaining components serve for address selection, which is described in the next section. To make the most of the pin compatibility of the PIA and the VIA, not everything is connected in the standard way. CS0 on PIAs is not used, because the VIA lacks this input.

PIAs need two address lines for register selection, VIAs four. Because RS2 and RS3 of

the VIA coincide with RS0 and RS1 of the PIA, for the PIA RS2 has been tied to A2 and RS3 to A3. The consequence is that each PIA register occupies four consecutive addresses, since A0 and A1 are not used for the PIA.

This use of the register select lines results in the arrangement of registers, shown in table 1, within the 16-address range assigned to a PIA or VIA. As an example, address C120 has been chosen for this address range.

Afb. 6 *Opwekken van het Kx-adresseselectiesignaal voor het gebied C000 tot en met C3FF.*



Selecting the PIA or VIA

The address decoding on the card has a resolution of 16 bytes. The VIA has 16 registers and itself decodes the address lines for these 16 bytes: A0 through A3. A PIA needs only four addresses, but for convenience is nevertheless allocated 16 addresses.

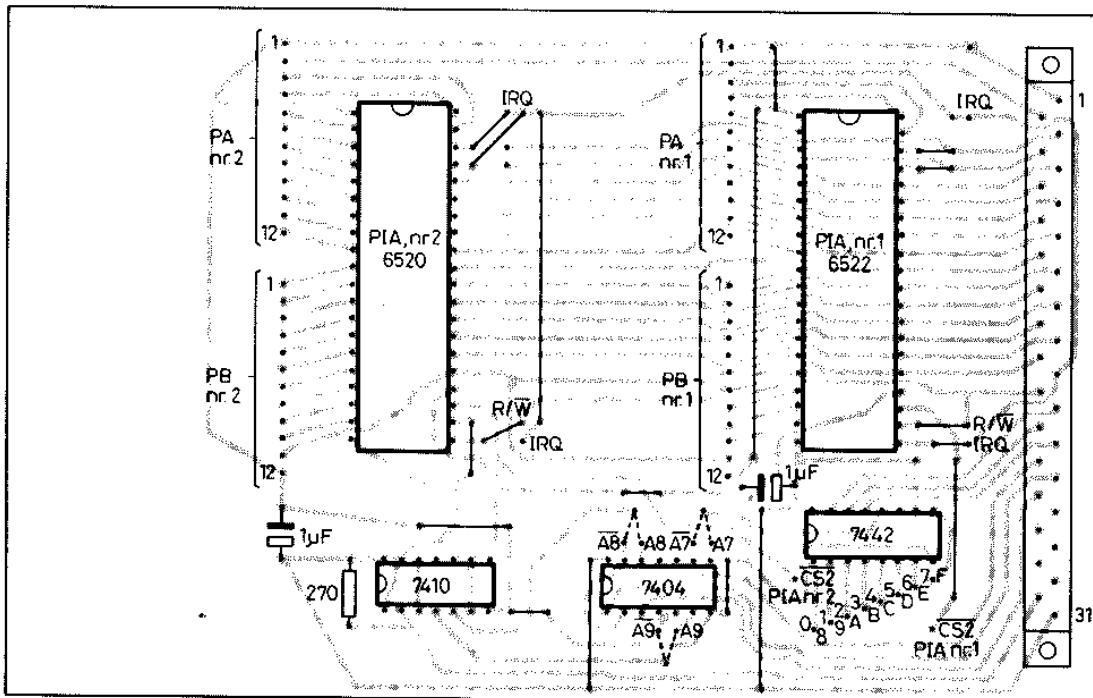
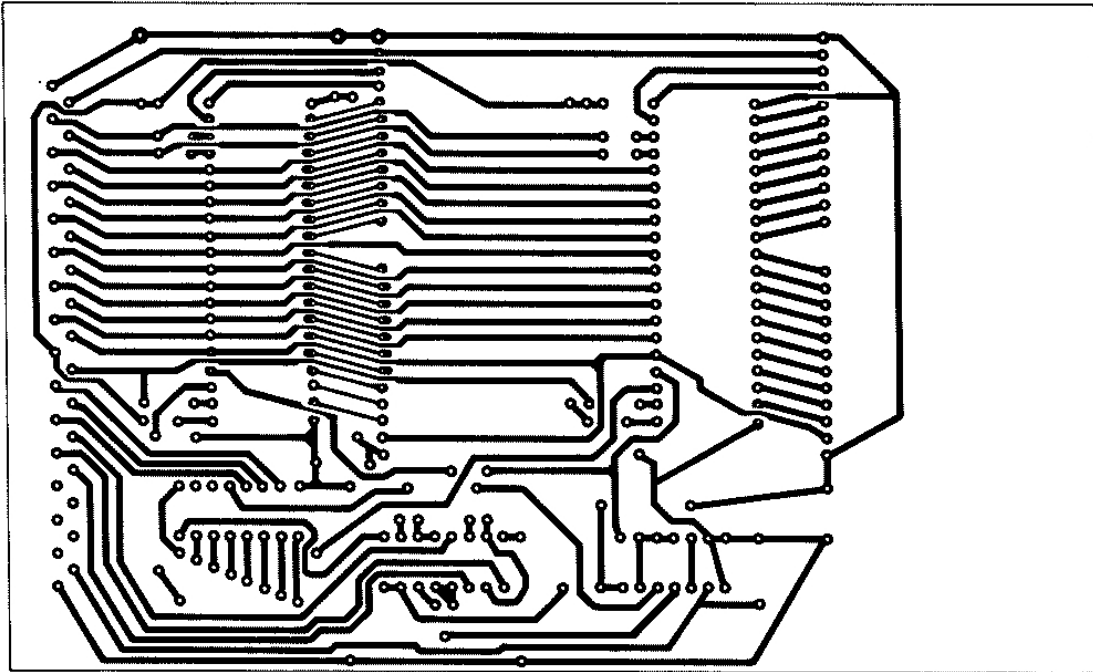
The start address of the registers can be set on the board with a number of wire jumpers. Address lines A4 through A9 are used for this, together with a signal Kx. The Kx signal selects a 1-Kbyte block by going low. Generating this Kx signal has been discussed before in Radio Bulletin, notably in connection with memory expansions for 6502 microprocessors. Fig. 6 shows a possible solution for generating a Kx signal from address lines A10 through A15.

To clarify how the wire jumpers are set, we will take an example: the start address C120. The wire jumpers are indicated on the component layout and in the schematic: the choice of one of the outputs of the decoder (7442), A7 or A7-not, A8 or A8-not, and A9 or A9-not. Table 2 shows how we break down the address and thereby choose the wire jumpers. The first digit (the least significant) is not involved in the address decoding; the VIA or PIA does that itself. The second digit is determined by A4 to A7. A4 to A6 are decoded by a type 7442 decoder, which thereby offers the choice of values 0...7 or 8...F for the second digit of the half address. Which of the two groups is chosen depends on A7. For the range 0...7 in the example, A7 and output 2 are required; this gives address C120. The third and fourth digits are determined by A8 and A9. Table 3 shows what the choice must be.

The example (see table 4) requires A8-not and A9 for address C120.

Once one of the PIAs or VIAs has been given an address in this way, that address is no

longer available to the second one. By choosing a different output of the 7442, the start address in the example can be set anywhere between C100 and C1F0.



PCB design

A PCB design has been made for the PIA/VIA card, shown in fig. 4. It is a single-sided board with Eurocard dimensions and a DIN41617 edge connector for the connections to the computer buses and supply lines. The inputs and outputs of the PIA or VIA are

available on the board. A flat ribbon cable can be soldered here or, as the board is designed for, a so-called mini-module connector. The header photo shows a prototype in which a front panel with mini-module connectors is connected to the board. The pin assignment of the board connector is given in table 5. This layout is the same as that of the previously published ACIA board.

The current consumption of the board is at most 250 mA at a 5 V supply voltage.

In addition to the A- or B-side connections of the PIA or VIA, including the control lines, the mini-module connectors also carry a ground line, the system clock $\phi 2$ (E) and an interrupt input (NMI). The arrangement can be seen in fig. 3.

Anyone who already needs more information about PIAs and VIAs is advised to study the manufacturers' documentation, or one of the books on the 6502 for the VIA, such as "6502 Assembly Language Programming" by Lance Leventhal, published by Osborne/McGraw-Hill.

Table 1 - Location of the PIA and VIA registers within their assigned memory range of 16 addresses.

Address	PIA register	VIA register
C000	DDRA/PRA	ORB (Output Register port B)
C001	(Data Direction Register A/	ORA (Output Register port A)
C002	Peripheral Register A)	DDRB (Data Direction Register B)
C003		DDRA (Data Direction Register A)
C004	CRA	T1L-L/C (Timer-1 Counter Low)
C005	(Control Register A)	T1CH (Timer-1 Counter High)
C006		T1L-L (Timer-1 Latch Low)
C007		T1L-H (Timer-1 Latch High)
C008	DDRB/PRB	T2L-L/T2C-L (Timer-2 Counter Low)
C009	(Data Direction Register B/	T2C-H (Timer-2 Counter High)
C00A	Peripheral Register B)	SR (Shift Register)
C00B		ACR (Auxiliary Control Register)
C00C	CRB	PCR (Peripheral Control Register)
C00D	(Control Register B)	IFR (Interrupt Flag Register)
C00E		IER (Interrupt Enable Register)
C00F		ORA (Output Register A)

address = X1 X2 X3 X4

```

_____ | |
         | | |
         | | |
         | | |
         | | |__ address lines A0 - A3, register selection
         | |
         | | _____ address lines A4 - A7
         |           A4, A5, A6 give a choice of 0 - 7 and 8 - F
         |           via an output of decoder IC 7442
         |           A7 selects from set 0 - 7
         |           A7-not selects from set 8 - F
         |
         | _____ address lines A8 and A9, and select line Kx

```

X000 - X3FF

X400 - X7FF

X800 – XBFF

XC00 – XFFF

A8 and A9 give a choice of: see table 3

Table 3 - Address selection of PIA and VIA.

A8	A9	X000...X0FF
A8-not	A9	X100...X1FF
A8	A9-not	X200...X2FF
A8-not	A9-not	X300...X3FF

Table 4 - Example of address selection.

address = C 1 2 0

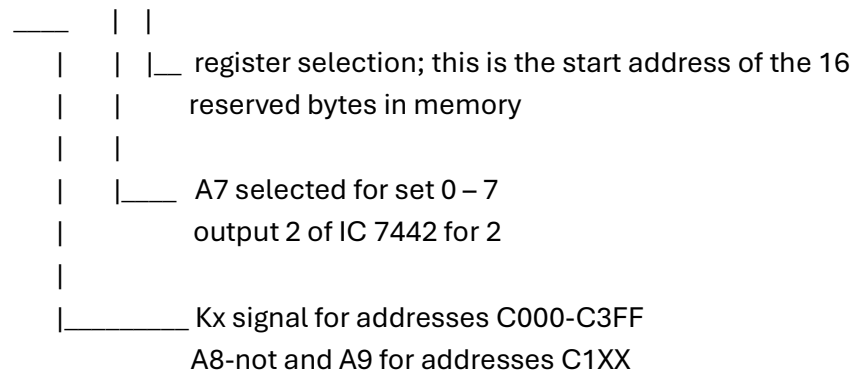


Table 5 - Pin assignment of the DIN41617 connector of the PIA/VIA board.

1 ground	17 IRQ
2 NMI	18 R/W
3 A0	19 A4
4 A1	20 A5
5 A2	21 A6
6 A3	22 A7
7 RESET	23 A8
8 D0	24 A9
9 D1	25 A10
10 D2	26 -5 V
11 D3	27 analog ground
12 D4	28 -12 V
13 D5	29 +12 V
14 D6	30 Kx
15 D7	31 +5 V
16	ϕ 2/E